



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,298	12/12/2003	Cheng-Wen Wu	B-5320 621551-4	9968

36716 7590 01/24/2006

LADAS & PARRY  
5670 WILSHIRE BOULEVARD, SUITE 2100  
LOS ANGELES, CA 90036-5679

EXAMINER
----------

BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
----------	--------------

2138

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/735,298	<b>Applicant(s)</b> WU ET AL.	
	<b>Examiner</b> Cynthia Britt	<b>Art Unit</b> 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 is/are allowed.
- 6) ☒ Claim(s) 5-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/12/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

### **DETAILED ACTION**

Claims 1-8 are presented for examination.

#### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on 12/12/03 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

#### ***Allowable Subject Matter***

Claims 1-4 are allowed.

#### ***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 5-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention is directed to non-statutory subject matter. (see MPEP 2106 IV B 1. (a) (p. 2100-13))

(a) Functional Descriptive Material: "Data Structures" Representing Descriptive Material

Art Unit: 2138

Per Se or Computer Programs Representing Computer Listings Per Se Data structures not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. ... Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

*"A Built-in Self-testing Method for Embedded Multiport Memory Arrays"* by Narayanan et al. Proceedings of the 21st IEEE Instrumentation and Measurement Technology Conference Publication Date: 18-20 May 2004 Vol 3, On pages 2027-2032 INSPEC Accession Number: 8083003

This paper teaches that multiport memories are widely used in multiprocessor systems, telecommunication ASICs etc. Research papers, which define multi-port memory fault models and give march tests for the same are currently available. However, little work, has been done to use the power of serial interfacing for testing multi-port memories. In this paper, we discuss some basics about the architecture of two-port memories and fault models for the same. We have then used the serial testing mechanism to propose new algorithms, which can prove effective to reduce the hardware cost considerably on a chip with many multi-port memories. Once the serial interfacing for two-port memory testing is understood, it can be extended for p-port memories ( $p > 2$ ). The proposed method based on the serial interfacing technique has the advantages of high fault coverage, low hardware overhead and tolerable test application time.

*"Realistic Fault Models and Test Procedure for Multi-port SRAMs"* by Hamdioui et al. IEEE International Workshop on Memory Technology, Design and Testing, Publication Date: 2001 On pages 65-72 INSPEC Accession Number: 7137971

Art Unit: 2138

This paper presents realistic fault models for multi-port memories with  $p$  ports, based on defect injection and SPICE simulation. The results show that the fault models for  $p$ -port memories consist of  $p$  classes: single-port faults, two-port faults, ... ,  $p$ -port faults. In addition, the paper discusses the test procedure for such memories. It shows that the time complexity of the required tests is not exponentially proportional with  $p$ , as published by different authors, but it is linear; irrespective of the number of ports in the multi-port memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Cynthia Britt  
Examiner  
Art Unit 2138